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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/895,991

06/29/2001

James W. Hofmann

Hofmann 1-51-15-7-4

9330

7590

11/01/2005

Theodore Naccarella  
Synnestvedt & Lechner LLP  
2600 Aramark Tower  
1101 Market Street  
Philadelphia, PA 19107-2950

EXAMINER

MEEK, JACOB M

ART UNIT

PAPER NUMBER

2637

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	09/895,991	HOFMANN ET AL.	
	Examiner	Art Unit	
	Jacob Meek	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1,3,5 - 10, 12 - 21, 23 - 37 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3,5 - 10, 12 - 21, 23 - 37 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1,3,5-10, 12 – 21, 23 - 37 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Objections***

2. Claim 24 is objected to because of the following informalities: Depends from cancelled claim 22. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 3, 5 - 10, and 12 - 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens (US Patent 6,173,345).

With regard to claim 1, Stevens discloses a method with (1) first device transmitting a bit pattern (see Figure 3, 315 where memory transfer accomplishes this result) to a second device responsive to a start signal transmitted from second device (see Figure 3, 315 where Read Signal initiates transfer); (2) second device sampling for bits of bit pattern sampling times determined as a function of a delay period after start signal (see figure 3, 320, and column 2, lines 26 - 35); (3) if second device does not detect said predetermined bit pattern,

increasing delay period and repeating as necessary (see figure 3, 320 NO branch); (4) if second device detects bit pattern, setting the last delay period used in step (2) as delay period to be used by second device for sampling data for further transmissions from first device to second device (see figure 3, 330 and column 7, lines 23 – 32); second device using said last delay period for sampling further data transmissions from said first device to said second device, wherein 2<sup>nd</sup> device performs step (2) twice before proceeding to steps 3 and 4 (see column 8, lines 20 - 37). Stevens is silent with respect to digital communications between two devices. Stevens discloses calculation of delay times of memory elements for data transfers in a processor-based system, but his technique would be operable for other peripheral devices relying on the transfer of data (digital communications), and therefore obvious to one of ordinary skill in the art.

With regard to claims 3, Stevens is silent with respect to start signal being a frame synchronization signal. Stevens discloses data transfer test is initiated via a READ signal (see column 6, line 65 – column 7, line 1). READ is a form of a data strobe signal used in processor based systems and is interpreted as providing equivalent functionality and therefore would have been obvious to one of ordinary skill in the art at the time of invention.

With regard to claim 5, Stevens discloses start signal is transmitted on a first signal line (see figure 2, 236 and column 4, lines 48 - 57), said predetermined pattern and all further data is transmitted on second signal lines (see Figure 2, 234 and column 4. lines 58 - 60) and a clock signal is generated on a third signal line (see figure 2, 232) and wherein transmissions on second signal line and sampling time are also a function of clock signal (see column 5, line 55 – column 6, line 4).

With regard to claim 6, Stevens discloses digital communication is carried out under control of a controller (see figure 2, 200) and is conducted between at least one target device

(see figure 2, 240 and column 4, lines 24 – 35 where data transfer is a basic form of digital communications).

With regard to claim 7, Stevens discloses start and clock signals are generated at 2<sup>nd</sup> device (see figure 2, 200,).

With regard to claim 8, Stevens discloses 1<sup>st</sup> device is one of target devices (see Figure 2, 240).

With regard to claim 9, Stevens discloses that 1<sup>st</sup> device transmits a predetermined bit pattern in response to receipt of an instruction from 2<sup>nd</sup> device (see figure 3. 315 and column 6, line 65 – column 7, line 1 predetermined pattern is set via write operation).

With regard to claim 10, Stevens discloses a method of delaying the data (see column 4, lines 36 – 38). Stevens discloses delaying in increments of one clock cycle but indicates other variable delays are useful (See column 4, lines 36 – 47). The selection of ½ delay is a basic clock offset and would have been an obvious delay increment due to ease of implementation.

With regard to claim 12, Stevens discloses the method of claim 1 (steps 1 – 5). Stevens is silent with respect to the transmission of data in anticipation of arrival of start signal. The transmission of data at a predicted time involves the simple use of timers. It would have obvious to one of ordinary skill in the art at the time of invention to transmit data at a known time instance, as this technique is well known in the art (TDMA).

With regard to claims 13 - 19, Stevens discloses a device incorporating the method of claims 1 – 10 as claimed above, and therefore would have been obvious considering the aforementioned rejection of claims 1 – 10.

With regard to claim 20, Stevens discloses a method of (1) receiving from a transmit device a predetermined bit pattern sent in response to a start signal (see figure 3, 315 where

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Read Signal initiates transfer), (2) sampling for bits of predetermined bit pattern a sampling times determined as a function of a delay period after a start signal (see figure 3, 320 and column 2, lines 26 - 35), (3) if predetermined bit pattern is not detected increasing delay period and repeating steps 1 & 2 (see figure 3, 320, NO branch), (4) if predetermined bit pattern is detected setting a last delay period used as delay period to be used for sampling data for further transmissions from transmit device (see figure 3, 330 and column 7, lines 23 – 32). Stevens is silent with respect to digital communications between two devices. Stevens discloses calculation of delay times of memory elements for data transfers in a processor-based system, but his technique would be operable for other peripheral devices relying on the transfer of data (digital communications), and therefore obvious to one of ordinary skill in the art.

With regard to claim 21, Stevens discloses the method of claim 20 (steps 1 – 5). Stevens is silent with respect to the transmission of data in anticipation of arrival of start signal. The transmission of data at a predicted time involves the simple use of timers. It would have obvious to one of ordinary skill in the art at the time of invention to transmit data at a known time instance, as this technique is well known in the art (TDMA).

With regard to claims 22 – 30, these method claims are analyzed in a similar manner to claims 2 – 10.

With regard to claims 31 - 37, Stevens teaches a device incorporating the method of claims 12, 22 – 29 as claimed above, and therefore would have been obvious considering the aforementioned rejection of claims 12, 22 – 29.

***Other Cited Prior Art***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Liu et al (US-6,725,390) discloses a method and apparatus to adjusting clock signal to sample data.

Jeddeloh (US-6,401,213) discloses a method and apparatus for the adjustment of sampling of data.

Gulick (US-6,279,058) discloses and apparatus and method for the clock control in a computer system.

Lafollette et al (US-6,212,171) discloses a method and apparatus for the determination of round trip delays in a communication system.

Collins et al (US-6,031,847) discloses a method and system for alignment of data.

Guo (US-5,367,542) discloses a method and system of data recovery utilizing  $\frac{1}{2}$  bit delay increments.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Meek whose telephone number is (571)272-3013. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571)272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMM  
10/28/05

*JMM*

TEMESGHEN GHEBRETTINSAE  
PRIMARY EXAMINER

TEMESGHEN GHEBRETTINSAE  
PRIMARY EXAMINER

10/31/05  
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